What is claimed is:

1. A ferroelectric random access memory (FeRAM) capacitor, comprising:

an active matrix including a semiconductor substrate, field oxide regions, a source/drain region, a first interlayer dielectric (ILD) and a storage node contact;

a capacitor stack including a bottom electrode, a ferroelectric layer and a top electrode, wherein the bottom electrode, the ferroelectric layer and the top electrode are formed on the active matrix and a width of the capacitor stack is relatively larger than that of the storage node;

a second ILD enclosing capacitor stack, wherein the top face of the top electrode is not covered with the second ILD; and

a plate line formed on the top face of the top electrode and predetermined portions of the second ILD, the width of the plate line being larger than that of the top electrode.

2. The FeRAM capacitor as recited in claim 1, further comprising:

a first glue layer formed between the first ILD and the bottom electrode; and

a second glue layer formed between the second ILD and the plate line.

3. The FeRAM capacitor as recited in claim 2, wherein

the first glue layer and the second glue layer employ alumina (Al_2O_3).

4. The FeRAM capacitor as recited in claim 3, wherein the first glue layer and the second glue layer are formed by using a method selected from the group consisting of an atomic layer deposition (ALD), a chemical mechanical polishing (CMP) and a physical vapor deposition (PVD).

5. The FeRAM capacitor as recited in claim 4, wherein the first glue layer and the second glue layer have the thickness in the range of about 5 Å to about 50 Å.

6. The FeRAM capacitor as recited in claim 1, wherein the top face of the top electrode is lower than the top face of the second ILD.

7. The FeRAM capacitor as recited in claim 1, wherein the second ILD uses a material selected from the group consisting of phosphorous silicate glass (PSG), spin-on-glass (SOG), undoped silicate glass (USG) and tetra-ethyl-ortho-silicate (TEOS).

8. The FeRAM capacitor as recited in claim 7, wherein the second ILD is a double layer in which a first layer is formed on the first ILD and sidewalls of the capacitor stack for preventing oxygen diffusion and a second layer is formed

on the first layer.

9. The FeRAM capacitor as recited in claim 8, wherein the first layer uses a material selected from the group consisting of titanium oxide (TiO_2), TEOS and Al_2O_3.

10. The FeRAM capacitor as recited in claim 8, wherein the second layer uses a material selected from the group consisting of PSG, SOG, USG and TEOS.

11. The FeRAM capacitor as recited in claim 1, wherein the bottom electrode is formed by using a method selected from the group consisting of the CVD, the PVD, the ALD and a plasma enhanced ALD (PEALD).

12. The FeRAM capacitor as recited in claim 11, wherein the bottom electrode employs a material selected from the group consisting of platinum (Pt), iridium (Ir), ruthenium (Ru), rhenium (Re), rhodium (Rh) and a combination thereof.

13. The FeRAM capacitor as recited in claim 1, wherein the ferroelectric layer is formed with the thickness in the range of about 50 Å to about 2,000 Å by using a method selected from the group consisting of a spin-on coating, the PVD, the CVD and the ALD.

14. The FeRAM capacitor as recited in claim 13, wherein

the ferroelectric layer uses a material selected from the group consisting of bismuth lanthanum titanate (BLT), strontium bismuth tantalate (SBT), strontium bismuth niobate tantalate (SBTN) and lead zirconate titanate (PZT).

15. The FeRAM capacitor as recited in claim 1, wherein the top electrode is formed with the thickness in the range of about 100 Å to about 1,000 Å by using a method selected from the group consisting of the CVD, the PVD, the ALD and the PEALD.

16. The FeRAM capacitor as recited in claim 15, wherein the top electrode uses a material selected from the group consisting of Pt, Ir, Ru, IrO2, RuO2, Pt/IrO_2, $Pt/IrO_2/Ir$, IrO_2/Ir, RuO_2/Ru, $Pt/RuO_2/Ru$ and Pt/RuO_2.

17. The FeRAM capacitor as recited in claim 1, wherein the plate line is formed with the thickness in the range of about 500 Å to about 3,000 Å by using a method selected from the group consisting of the PVD, the CVD and the ALD.

18. A method for manufacturing a ferroelectric random access memory (FeRAM) capacitor, the method comprising the steps of:

a) preparing an active matrix including a semiconductor substrate, a source/drain region, FOX regions, a first ILD, a storage node contact;

b) forming a first conductive layer, a dielectric layer and a second conductive layer on the active matrix in sequence;

c) forming a hard mask on a predetermined location of the second conductive layer;

d) patterning the second conductive layer, the dielectric layer and the first conductive layer by using the hard mask, thereby forming a capacitor stack having a bottom electrode, a ferroelectric layer and a top electrode, a width of the capacitor stack being larger than that of the storage node contact;

e) forming a second ILD on the first ILD and the hard mask, wherein the second ILD embraces the capacitor stack;

f) planarizing the second ILD till the top face of the hard mask is exposed;

g) removing the hard mask to form an opening above the top electrode; and

h) forming a third conductive layer over the resultant structure and patterning into a predetermined configuration, thereby obtaining a plate line of which a width is larger than that of the capacitor stack, the plate line being electrically connected to the top electrode.

19. The method as recited in claim 18, before the step b), further comprising the step of forming a first glue layer between the first ILD and the first conductive layer.

20. The method as recited in claim 19, wherein the first glue layer uses Al_2O_3.

21. The method as recited in claim 19, wherein the step of forming the first glue layer is carried out by using a method selected from the group consisting of an ALD, a CVD and the a PVD.

22. The method as recited in claim 19, wherein the first glue layer has the thickness in a range of about 5 Å to about 50 Å.

23. The method as recited in claim 18, wherein the step c) includes the steps of:

c1) forming a hard mask layer on the second conductive layer;

c2) forming a photoresist layer on the hard mask layer and patterning the photoresist layer into a preset configuration, thereby obtaining a photoresist pattern; and

c3) forming the hard mask by patterning the hard mask layer into a predetermined configuration by using the photoresist pattern as a mask.

24. The method as recited in claim 23, wherein the hard mask uses a titanium nitride (TiN).

25. The method as recited in claim 23, wherein the hard

mask uses a tantalum nitride (TaN).

26. The method as recited in claim 18, wherein the hard mask layer is formed by using a method selected from the group consisting of the PVD, the CVD and the ALD.

27. The method as recited in claim 18, wherein the step f) is carried out by using the CMP process.

28. The method as recited in claim 18, wherein the step f) is carried out by using an etchback process.

29. The method as recited in claim 18, wherein the step f) is carried out by using an etchback process after carrying out the CMP process.

30. The method as recited in claim 18, wherein the second ILD uses a material selected from the group consisting of PSG, SOG and USG.

31. The method as recited in claim 30, wherein the step e) includes the steps of:

e1) forming a first layer on the top face of the first ILD and side walls of the capacitor stack for preventing oxygen diffusion; and

e2) forming a second layer on the first ILD.

32. The method as recited in claim 31, wherein the first layer uses a material selected from the group consisting of TiO_2, TEOS and Al_2O_3 and the second layer uses a material selected from the group consisting of PSG, SOG and USG.

33. The method as recited in claim 18, after the step e) further comprising the step of carrying out a curing process for removing moisture in the second ILD and densifying the second ILD.

34. The method as recited in claim 33, wherein the curing process is carried out in an ambient of gas selected from the group consisting of oxygen (O_2), nitrogen (N_2) and argon for about ten minutes to about 2 hours at a temperature below about 550 ℃.

35. The method as recited in claim 18, wherein the step g) is carried out by using a wet etching process.

36. The method as recited in claim 35, wherein the wet etching process is carried out by using a mixed solution of which NH_4OH, H_2O_2 and H_2O are mixed in a ratio of about 1 to about 4 to about 20.

37. The method as recited in claim 18, wherein the step g) is carried out by using a dry etching process.

38. The method as recited in claim 37, wherein the dry etching process is carried out by using a mixed gas of argon (Ar) and chlorine (Cl_2).

39. The method as recited in claim 18, before the step h), further comprising the step of forming a second glue layer between the second ILD and the third conductive layer.

40. The method as recited in claim 39, wherein the second glue layer uses Al_2O_3.

41. The method as recited in claim 39, wherein the step of forming the second glue layer is carried out by using a method selected from the group consisting of the ALD, the CVD and the PVD.

42. The method as recited in claim 39, wherein the second glue layer has the thickness in the range of about 5 Å to about 50 Å.

43. The method as recited in claim 18, wherein the first conductive layer is formed with the thickness in the range of about 100 Å to 1,000 Å by using a method selected from the group consisting of the CVD, the PVD, the ALD and a PEALD.

44. The method as recited in claim 43, wherein the first

conductive layer employs a material selected from the group consisting of Pt, Ir, Ru, Re, Rh and a combination thereof.

45. The method as recited in claim 18, wherein the dielectric layer is formed with the thickness in the range of about 50 Å to about 2,000 Å by using a method selected from the group consisting of a spin-on coating, the PVD, the CVD and the ALD.

46. The method as recited in claim 45, wherein the dielectric layer uses a ferroelectric material selected from the group consisting of BLT, SBT, SBTN and PZT.

47. The method as recited in claim 18, wherein the second conductive layer is formed with the thickness in the range of about 100 Å to about 1,000 Å by using a method selected from the group consisting of the CVD, the PVD, the ALD and the PEALD.

48. The method as recited in claim 47, wherein the second conductive layer uses a material selected from the group consisting of Pt, Ir, Ru, IrO_2, RuO_2, Pt/IrO_2, $Pt/IrO_2/Ir$, IrO_2/Ir, RuO_2/Ru, $Pt/RuO_2/Ru$ and Pt/RuO_2.

49. The method as recited in claim 18, wherein the third conductive layer is formed with the thickness in the range of

about 500 Å to about 3,000 Å by using a method selected from the group consisting of the PVD, the CVD and the ALD.